

## **DDR3/L S Series Datasheet**

**RONSYN ELECTRONICS (HONG KONG) LIMITED**

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**Revision History**

| Revision No. | History                                   | Date      | Remark |
|--------------|-------------------------------------------|-----------|--------|
| 0.1          | Preliminary                               | Jun. 2025 |        |
| 0.2          | Add x8 config                             | Aug. 2025 |        |
| 0.3          | Add DEC3L2AAS08D18F2                      | Aug. 2025 |        |
| 0.4          | Add DECD32AAS08D18F2,<br>DECD32AAS08D10F7 | Sep. 2025 |        |
|              |                                           |           |        |
|              |                                           |           |        |
|              |                                           |           |        |
|              |                                           |           |        |

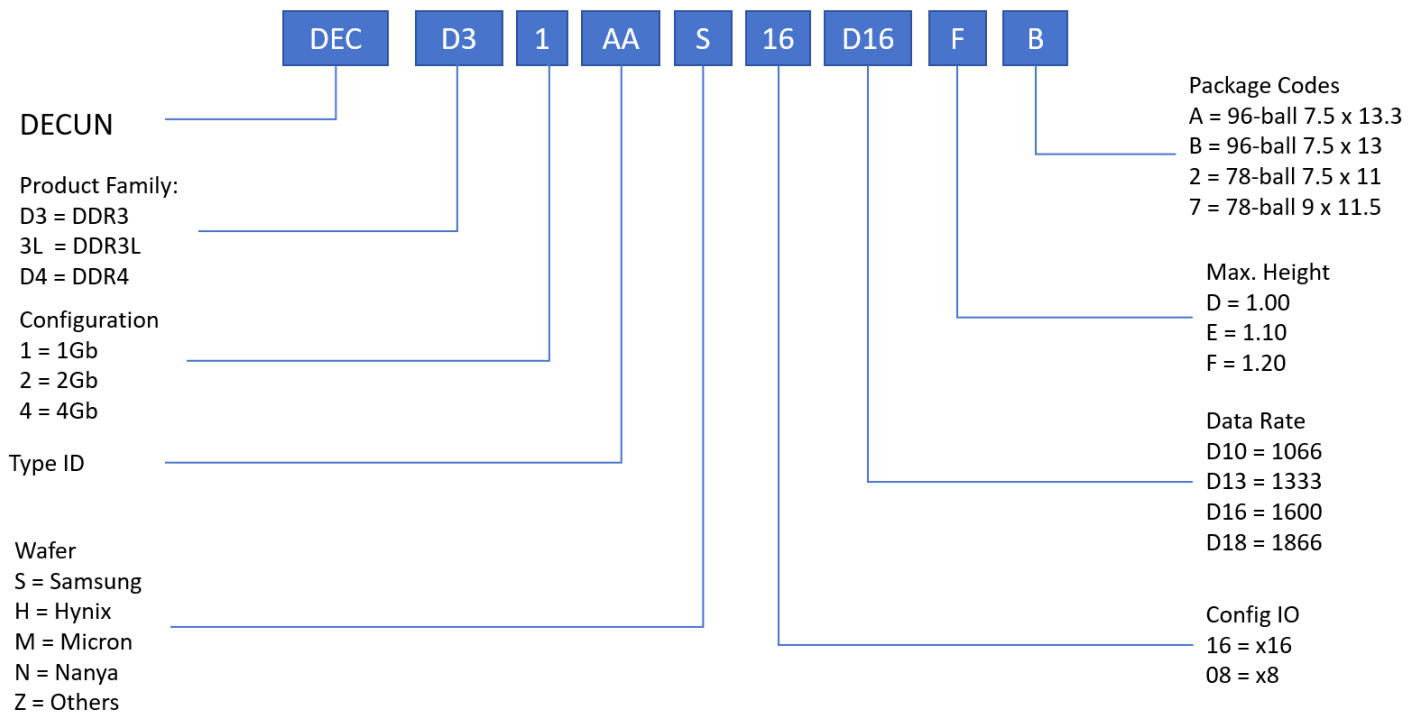
## Device Features and Ordering Information

### FEATURES

- SSTL\_135 for DDR3L: VDD/VDDQ=1.35V(-0.067/+0.1V)
- SSTL\_15 for DDR3: VDD/VDDQ=1.5V(±0.075V)
- 8 Banks
- Posted CAS
- Programmable CAS Latency(posted CAS): 6,7,8,9,10,11,12,13
- Programmable Additive Latency: 0, CL-2 or CL-1 clock
- Programmable CAS Write Latency: (CWL) =6,7, 8, 9,10
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data-Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
- On Die Termination using ODT pin
- Average Refresh Period: 7.8us at lower than TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C
- Asynchronous Reset
- Package : 96 balls FBGA - x16, 78 balls FBGA - x8
- All of Lead-Free products are compliant for RoHS
- All of products are Halogen-Free

### Part Number Ordering Information

#### Part Number Chart



## Part Number List

| Part No.         | Configuration | Max Speed           | Total Density | Package     |
|------------------|---------------|---------------------|---------------|-------------|
| <b>DDR3 x16</b>  |               |                     |               |             |
| DECD31AAS16D16FA | 64M x 16      | DDR3-1600 11-11-11  | 1Gb           | 96ball FBGA |
| DECD31AAS16D18FA | 64M x 16      | DDR3-1866 13-13-13  | 1Gb           | 96ball FBGA |
| <b>DDR3 x8</b>   |               |                     |               |             |
| DECD31AAS08D10F2 | 128M x 8      | DDR3-1066 7-7-7     | 1Gb           | 78ball FBGA |
| DECD31AAS08D13F2 | 128M x 8      | DDR3-1333 9-9-9     | 1Gb           | 78ball FBGA |
| DECD31AAS08D16F2 | 128M x 8      | DDR3-1600 11-11-11  | 1Gb           | 78ball FBGA |
| DECD32AAS08D10F2 | 256M x 8      | DDR3-1066 7-7-7     | 2Gb           | 78ball FBGA |
| DECD32AAS08D10F7 | 256M x 8      | DDR3-1066 7-7-7     | 2Gb           | 78ball FBGA |
| DECD32AAS08D13F2 | 256M x 8      | DDR3-1333 9-9-9     | 2Gb           | 78ball FBGA |
| DECD32AAS08D16F2 | 256M x 8      | DDR3-1600 11-11-11  | 2Gb           | 78ball FBGA |
| DECD32AAS08D18F2 | 256M x 8      | DDR3-1866 13-13-13  | 2Gb           | 78ball FBGA |
| <b>DDR3L x8</b>  |               |                     |               |             |
| DEC3L1AAS08D13F2 | 128M x 8      | DDR3L-1333 9-9-9    | 1Gb           | 78ball FBGA |
| DEC3L2AAS08D10F2 | 256M x 8      | DDR3L-1066 7-7-7    | 2Gb           | 78ball FBGA |
| DEC3L2AAS08D13F2 | 256M x 8      | DDR3L-1333 9-9-9    | 2Gb           | 78ball FBGA |
| DEC3L2AAS08D16F2 | 256M x 8      | DDR3L-1600 11-11-11 | 2Gb           | 78ball FBGA |
| DEC3L2AAS08D18F2 | 256M x 8      | DDR3L-1866 13-13-13 | 2Gb           | 78ball FBGA |

## Package Ballout

### x16 Package Ball out (Top view): 96ball FBGA Package

|   | 1      | 2                         | 3                        | 4 | 5 | 6 | 7                               | 8      | 9    |   |
|---|--------|---------------------------|--------------------------|---|---|---|---------------------------------|--------|------|---|
| A | VDDQ   | DQU5                      | DQU7                     |   |   |   | DQU4                            | VDDQ   | VSS  | A |
| B | VSSQ   | VDD                       | VSS                      |   |   |   | $\overline{\text{DQS}}\text{U}$ | DQU6   | VSSQ | B |
| C | VDDQ   | DQU3                      | DQU1                     |   |   |   | DQSU                            | DQU2   | VDDQ | C |
| D | VSSQ   | VDDQ                      | DMU                      |   |   |   | DQU0                            | VSSQ   | VDD  | D |
| E | VSS    | VSSQ                      | DQL0                     |   |   |   | DML1                            | VSSQ   | VDDQ | E |
| F | VDDQ   | DQL2                      | DQSL                     |   |   |   | DQL1                            | DQL3   | VSSQ | F |
| G | VSSQ   | DQL6                      | $\overline{\text{DQSL}}$ |   |   |   | VDD                             | VSS    | VSSQ | G |
| H | VREFDQ | VDDQ                      | DQL4                     |   |   |   | DQL7                            | DQL5   | VDDQ | H |
| J | NC     | VSS                       | $\overline{\text{RAS}}$  |   |   |   | CK                              | VSS    | NC   | J |
| K | ODT    | VDD                       | $\overline{\text{CAS}}$  |   |   |   | $\overline{\text{CK}}$          | VDD    | CKE  | K |
| L | NC     | $\overline{\text{CS}}$    | $\overline{\text{WE}}$   |   |   |   | A10/AP                          | ZQ     | NC   | L |
| M | VSS    | BA0                       | BA2                      |   |   |   | NC                              | VREFCA | VSS  | M |
| N | VDD    | A3                        | A0                       |   |   |   | A12/ $\overline{\text{BC}}$     | BA1    | VDD  | N |
| P | VSS    | A5                        | A2                       |   |   |   | A1                              | A4     | VSS  | P |
| R | VDD    | A7                        | A9                       |   |   |   | A11                             | A6     | VDD  | R |
| T | VSS    | $\overline{\text{RESET}}$ | A13                      |   |   |   | NC                              | A8     | VSS  | T |

### Ball Locations(x16)

- Populate ball
- Ball not populated

### Top view

(See the balls through the package)

|   | 1 | 2 | 3 |  | 7 | 8 | 9 |
|---|---|---|---|--|---|---|---|
| A | ● | ● | ● |  | ● | ● | ● |
| B | ● | ● | ● |  | ● | ● | ● |
| C | ● | ● | ● |  | ● | ● | ● |
| D | ● | ● | ● |  | ● | ● | ● |
| E | ● | ● | ● |  | ● | ● | ● |
| F | ● | ● | ● |  | ● | ● | ● |
| G | ● | ● | ● |  | ● | ● | ● |
| H | ● | ● | ● |  | ● | ● | ● |
| J | ● | ● | ● |  | ● | ● | ● |
| K | ● | ● | ● |  | ● | ● | ● |
| L | ● | ● | ● |  | ● | ● | ● |
| M | ● | ● | ● |  | ● | ● | ● |
| N | ● | ● | ● |  | ● | ● | ● |
| P | ● | ● | ● |  | ● | ● | ● |
| R | ● | ● | ● |  | ● | ● | ● |
| T | ● | ● | ● |  | ● | ● | ● |

## x8 Package Ball out (Top view): 78ball FBGA Package

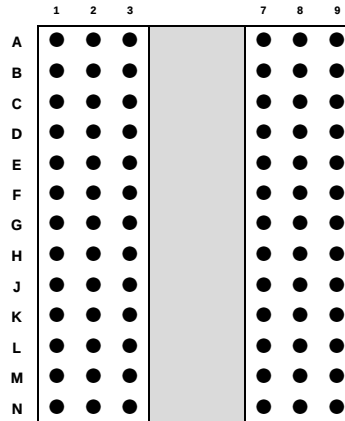
|   | 1      | 2                         | 3                       | 4 | 5 | 6 | 7                            | 8      | 9    |   |
|---|--------|---------------------------|-------------------------|---|---|---|------------------------------|--------|------|---|
| A | VSS    | VDD                       | NC                      |   |   |   | NU, $\overline{\text{TDQS}}$ | VSS    | VDD  | A |
| B | VSS    | VSSQ                      | DQ0                     |   |   |   | DM, $\text{TDQS}$            | VSSQ   | VDDQ | B |
| C | VDDQ   | DQ2                       | DQS                     |   |   |   | DQ1                          | DQ3    | VSSQ | C |
| D | VSSQ   | DQ6                       | $\overline{\text{DQS}}$ |   |   |   | VDD                          | VSS    | VSSQ | D |
| E | VREFDQ | VDDQ                      | DQ4                     |   |   |   | DQ7                          | DQ5    | VDDQ | E |
| F | NC     | VSS                       | $\overline{\text{RAS}}$ |   |   |   | CK                           | VSS    | NC   | F |
| G | ODT    | VDD                       | $\overline{\text{CAS}}$ |   |   |   | $\overline{\text{CK}}$       | VDD    | CKE  | G |
| H | NC     | $\overline{\text{CS}}$    | $\overline{\text{WE}}$  |   |   |   | A10/AP                       | ZQ     | NC   | H |
| J | VSS    | BA0                       | BA2                     |   |   |   | NC                           | VREFCA | VSS  | J |
| K | VDD    | A3                        | A0                      |   |   |   | A12/ $\overline{\text{BC}}$  | BA1    | VDD  | K |
| L | VSS    | A5                        | A2                      |   |   |   | A1                           | A4     | VSS  | L |
| M | VDD    | A7                        | A9                      |   |   |   | A11                          | A6     | VDD  | M |
| N | VSS    | $\overline{\text{RESET}}$ | A13                     |   |   |   | NC                           | A8     | VSS  | N |

### Ball Locations(x8)

- Populate ball
- Ball not populated

### Top view

(See the balls through the package)



## Pin Functional Descriptions

| Symbol                                                   | Type  | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|----------------------------------------------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CK, $\overline{CK}$                                      | Input | Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$ .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| CKE                                                      | Input | Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ , ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh. |
| $\overline{CS}$                                          | Input | Chip Select: All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| ODT                                                      | Input | On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS and DM/TDQS, NU/TDQS (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU, DQSL, DQSL, DMU, and DML signal. The ODT pin will be ignored if MR1 is programmed to disable ODT.                                                                                                                                                                                                                                                                                     |
| $\overline{RAS}$ ,<br>$\overline{CAS}$ , $\overline{WE}$ | Input | Command Inputs: $\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$ ) define the command being entered.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| DM<br>(DMU),(DML)                                        | Input | Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/TDQS is enabled by Mode Register A11 setting in MR1.                                                                                                                                                                                                                                                                                                                                                                                                                 |
| BA0 - BA2                                                | Input | Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| A0 - A14                                                 | Input | Address Inputs: Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC have additional functions, see below). The address inputs also provide the op-code during Mode Register Set commands.                                                                                                                                                                                                                                                                                                                                                                                         |
| A10 / AP                                                 | Input | Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.                                                                                                                                                                                                                                                                              |
| A12 / $\overline{BC}$                                    | Input | Burst Chop: A12 / $\overline{BC}$ is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| $\overline{RESET}$                                       | Input | Active Low Asynchronous Reset: Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

| Symbol                  | Type           | Function                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------------------------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                         |                | operation.<br>$\overline{RESET}$ is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V for DC low.                                                                                                                                                                                                                                                           |
| DQ                      | Input / Output | Data Input/ Output: Bi-directional data bus.                                                                                                                                                                                                                                                                                                                                                                      |
| DQS, $\overline{DQS}$   | Input / Output | Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data.                                                                                                                                                                                                                                                                                                   |
| TDQS, $\overline{TDQS}$ | Output         | Termination Data Strobe: TDQS/ $\overline{TDQS}$ is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/ $\overline{TDQS}$ that is applied to DQS/ $\overline{DQS}$ . When disabled via mode register A11 = 0 in MR1, DM/ $\overline{TDQS}$ will provide the data mask function and $\overline{TDQS}$ is not used. |
| NC                      |                | No Connect: No internal electrical connection is present.                                                                                                                                                                                                                                                                                                                                                         |
| VDDQ                    | Supply         | DQ Power Supply: 1.35V(1.28V~1.45V) , 1.5V(1.425V~1.575V)                                                                                                                                                                                                                                                                                                                                                         |
| VSSQ                    | Supply         | DQ Ground                                                                                                                                                                                                                                                                                                                                                                                                         |
| VDD                     | Supply         | Power Supply: 1.35V(1.28V~1.45V) , 1.5V(1.425V~1.575V)                                                                                                                                                                                                                                                                                                                                                            |
| VSS                     | Supply         | Ground                                                                                                                                                                                                                                                                                                                                                                                                            |
| VREFDQ                  | Supply         | Reference voltage for DQ                                                                                                                                                                                                                                                                                                                                                                                          |
| VREFCA                  | Supply         | Reference voltage for CA                                                                                                                                                                                                                                                                                                                                                                                          |
| ZQ                      | Supply         | Reference Pin for ZQ calibration                                                                                                                                                                                                                                                                                                                                                                                  |

**Note:**

Input only pins (BA0-BA2, A0-A14,  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ ,  $\overline{CS}$ , CKE, ODT and  $\overline{RESET}$ ) do not supply termination.



## ROW AND COLUMN ADDRESS TABLE

### 1Gb

| Configuration          | 128Mb x 8            | 64Mb x 16            |
|------------------------|----------------------|----------------------|
| # of Banks             | 8                    | 8                    |
| Bank Address           | BA0 - BA2            | BA0 - BA2            |
| Auto precharge         | A10/AP               | A10/AP               |
| BL switch on the fly   | A12/ $\overline{BC}$ | A12/ $\overline{BC}$ |
| Row Address            | A0 - A13             | A0 - A12             |
| Column Address         | A0 - A9              | A0 - A9              |
| Page size <sup>1</sup> | 1 KB                 | 2 KB                 |

### 2Gb

| Configuration          | 256Mb x 8            | 128Mb x 16           |
|------------------------|----------------------|----------------------|
| # of Banks             | 8                    | 8                    |
| Bank Address           | BA0 - BA2            | BA0 - BA2            |
| Auto precharge         | A10/AP               | A10/AP               |
| BL switch on the fly   | A12/ $\overline{BC}$ | A12/ $\overline{BC}$ |
| Row Address            | A0 - A14             | A0 - A13             |
| Column Address         | A0 - A9              | A0 - A9              |
| Page size <sup>1</sup> | 1 KB                 | 2 KB                 |

**Note1:** Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows:

$$\text{page size} = 2^{\text{COLBITS}} * \text{ORG} \div 8$$

where COLBITS = the number of column address bits, ORG = the number of I/O (DQ) bits

## Absolute Maximum Ratings

### Absolute Maximum DC Ratings

#### Absolute Maximum DC Ratings

| Symbol                             | Parameter                           | Rating            | Units | Notes |
|------------------------------------|-------------------------------------|-------------------|-------|-------|
| VDD                                | Voltage on VDD pin relative to Vss  | - 0.4 V ~ 1.975 V | V     | 1,3   |
| VDDQ                               | Voltage on VDDQ pin relative to Vss | - 0.4 V ~ 1.975 V | V     | 1,3   |
| V <sub>IN</sub> , V <sub>OUT</sub> | Voltage on any pin relative to Vss  | - 0.4 V ~ 1.975 V | V     | 1     |
| T <sub>STG</sub>                   | Storage Temperature                 | -55 to +100       | °C    | 1, 2  |

#### Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6XVDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

## DRAM Component Operating Temperature Range

### Temperature Range

| Symbol            | Parameter                             | Rating   | Units | Notes |
|-------------------|---------------------------------------|----------|-------|-------|
| T <sub>OPER</sub> | Normal Operating Temperature Range    | 0 to 85  | °C    | 1,2   |
|                   | Extended Temperature Range (Optional) | 85 to 95 | °C    | 1,3   |

#### Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JEDEC51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are supported in this range, but the following additional conditions apply:
  - a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range.  
Please refer to the DIMM SPD for option availability
  - b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

## AC & DC Operating Conditions

### Recommended DC Operating Conditions

#### Recommended DC Operating Conditions

| Symbol | Parameter                 | Operation Voltage | Rating |       |        | Units | Notes |
|--------|---------------------------|-------------------|--------|-------|--------|-------|-------|
|        |                           |                   | Min.   | Typ.  | Max.   |       |       |
| VDD    | Supply Voltage            | 1.35V             | 1.283  | 1.35  | 1.4500 | V     | 1,2,3 |
|        |                           | 1.5V              | 1.425  | 1.500 | 1.575  | V     | 1,2,3 |
| VDDQ   | Supply Voltage for Output | 1.35V             | 1.283  | 1.35  | 1.4500 | V     | 1,2,3 |
|        |                           | 1.5V              | 1.425  | 1.500 | 1.575  | V     | 1,2,3 |

#### Notes:

1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. VDD & VDDQ rating are determined by operation voltage.

## IDD and IDDQ Specification Parameters and Test Conditions

### IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure 1. shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- "0" and "LOW" is defined as  $V_{IN} \leq V_{ILAC(max)}$ .
- "1" and "HIGH" is defined as  $V_{IN} \geq V_{IHAC(min)}$ .
- "MID\_LEVEL" is defined as inputs are  $V_{REF} = V_{DD}/2$ .
- Timing used for IDD and IDDQ Measurement-Loop Patterns are provided in Table 1.
- Basic IDD and IDDQ Measurement Conditions are described in Table 2.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 3 through Table 10.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting  
 $R_{ON} = R_{ZQ}/7$  (34 Ohm in MR1);  
 $Q_{off} = 0_B$  (Output Buffer enabled in MR1);  $RTT_{Nom} = R_{ZQ}/6$  (40 Ohm in MR1);  
 $RTT_{Wr} = R_{ZQ}/2$  (120 Ohm in MR2);  
 TDQS Feature disabled in MR1
- Attention: The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define  $D = \{\overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE}\} := \{HIGH, LOW, LOW, LOW\}$
- Define  $\overline{D} = \{\overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE}\} := \{HIGH, HIGH, HIGH, HIGH\}$

**Table 1 -Timings used for IDD and IDDQ Measurement-Loop Patterns**

| Symbol          |     | DDR3-1066 | DDR3-1333 | DDR3-1600 | DDR3-1866 | Unit |
|-----------------|-----|-----------|-----------|-----------|-----------|------|
|                 |     | 7-7-7     | 9-9-9     | 11-11-11  | 13-13-13  |      |
| $t_{CK}$        |     | 1.875     | 1.5       | 1.25      | 1.07      | ns   |
| CL              |     | 7         | 9         | 11        | 13        | nCK  |
| $n_{RCD}$       |     | 7         | 9         | 11        | 13        | nCK  |
| $n_{RC}$        |     | 27        | 33        | 39        | 45        | nCK  |
| $n_{RAS}$       |     | 20        | 24        | 28        | 32        | nCK  |
| $n_{RP}$        |     | 7         | 9         | 11        | 13        | nCK  |
| $n_{FAW}$       | x8  | 20        | 20        | 24        | 26        | nCK  |
|                 | x16 | 27        | 30        | 32        | 33        | nCK  |
| $n_{RRD}$       | x8  | 4         | 4         | 5         | 5         | nCK  |
|                 | x16 | 6         | 5         | 6         | 6         | nCK  |
| $n_{REC}$ -1 Gb |     | 59        | 74        | 88        | 103       | nCK  |
| $n_{REC}$ -2 Gb |     | 86        | 107       | 128       | 150       | nCK  |

**Table 2 -Basic IDD and IDDQ Measurement Conditions**

| Symbol    | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $I_{DD0}$ | <p><b>Operating One Bank Active-Precharge Current</b></p> <p>CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 1; BL: 8<sup>a</sup>; AL: 0; <math>\overline{CS}</math>: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to Table 3; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 3); Output Buffer and RTT: Enabled in Mode Registers<sup>b</sup>); ODT Signal: stable at 0; Pattern Details: see Table 3.</p> |
| $I_{DD1}$ | <p><b>Operating One Bank Active-Read-Precharge Current</b></p> <p>CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 1; BL: 8<sup>a</sup>; AL: 0; CS: High between ACT, RD and PRE; Command, Address; Bank Address Inputs, Data IO: partially toggling according to Table 4; DM: stable at 0; Bank Activity: Cycling with on bank active at a time: 0,0,1,1,2,2,... (see Table 4); Output Buffer and RTT: Enabled in Mode Registers<sup>b</sup>); ODT Signal: stable at 0; Pattern Details: see Table 4.</p>                      |

|             |                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $I_{DD2N}$  | <b>Precharge Standby Current</b><br>CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0;<br>Pattern Details: see Table 5.                       |
| $I_{DD2NT}$ | <b>Precharge Standby ODT Current</b><br>CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 6; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: toggling<br>according to Table 6; Pattern Details: see Table 6. |
| $I_{DD2P0}$ | <b>Precharge Power-Down Current Slow Exit</b><br>CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0; Precharge Power Down<br>Mode: Slow Exit <sup>c)</sup>                  |
| $I_{DD2P1}$ | <b>Precharge Power-Down Current Fast Exit</b><br>CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0; Precharge Power Down<br>Mode: Fast Exit <sup>c)</sup>                  |
| $I_{DD2Q}$  | <b>Precharge Quiet Standby Current</b><br>CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed;<br>Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0                                                                            |
| $I_{DD3N}$  | <b>Active Standby Current</b><br>CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0;<br>Pattern Details: see Table 5.                            |

|            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $I_{DD3P}$ | <b>Active Power-Down Current</b><br>CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks open;<br>Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0                                                                                                                                                                                                                                 |
| $I_{DD4R}$ | <b>Operating Burst Read Current</b><br>CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : High between RD; Command, Address, Bank Address Inputs: partially toggling according to Table 7; Data IO: seamless read data burst with different data between one burst and the next one according to Table 7; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...(see Table 7); Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0; Pattern Details: see Table 7.     |
| $I_{DD4W}$ | <b>Operating Burst Write Current</b><br>CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : High between WR; Command, Address, Bank Address Inputs: partially toggling according to Table 8; Data IO: seamless read data burst with different data between one burst and the next one according to Table 8; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...(see Table 8); Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at HIGH; Pattern Details: see Table 8. |
| $I_{DD5B}$ | <b>Burst Refresh Current</b><br>CKE: High; External clock: On; tCK, CL, nRFC: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ : High between REF; Command, Address, Bank Address Inputs: partially toggling according to Table 9; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: REF command every nREC (see Table 9); Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: stable at 0; Pattern Details: see Table 9.                                                                                                                                           |
| $I_{DD6}$  | <b>Self-Refresh Current: Normal Temperature Range</b><br>$T_{CASE}$ : 0 - 85 °C; Auto Self-Refresh (ASR): Disabled <sup>d)</sup> ; Self-Refresh Temperature Range (SRT): Normal <sup>e)</sup> ; CKE: Low; External clock: Off; CK and $\overline{CK}$ : LOW; CL: see Table 1; BL: 8 <sup>a)</sup> ; AL: 0; $\overline{CS}$ , Command, Address, Bank Address Inputs, Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers <sup>b)</sup> ; ODT Signal: MID-LEVEL                                                                  |

|               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>/DD6ET</b> | <p><b>Self-Refresh Current: Extended Temperature Range</b></p> <p><math>T_{CASE}</math>: 0 - 95 °C; Auto Self-Refresh (ASR): Disabled<sup>d)</sup>; Self-Refresh Temperature Range (SRT): Extended<sup>e)</sup>; CKE: Low; External clock: Off; CK and <math>\overline{CK}</math>: LOW; CL: see Table 1; BL: 8<sup>a)</sup>; AL: 0; <math>\overline{CS}</math>, Command, Address, Bank Address Inputs, Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers<sup>b)</sup>; ODT Signal: MID-LEVEL</p>                                                     |
| <b>/DD6TC</b> | <p><b>Auto Self-Refresh Current</b></p> <p><math>T_{CASE}</math>: 0 - 95 °C; Auto Self-Refresh (ASR): Enabled<sup>d)</sup>; Self-Refresh Temperature Range (SRT): Normal<sup>e)</sup>; CKE: Low; External clock: Off; CK and <math>\overline{CK}</math>: LOW; CL: see Table 1; BL: 8<sup>a)</sup>; AL: 0; <math>\overline{CS}</math>, Command, Address, Bank Address Inputs, Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers<sup>b)</sup>; ODT Signal: MID-LEVEL</p>                                                                                               |
| <b>/DD7</b>   | <p>Operating Bank Interleave Read Current</p> <p>CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, NRRD, nFAW, CL: see Table 1; BL: 8<sup>a)f)</sup>; AL: CL-1; CS: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling according to Table 10; Data IO: read data burst with different data between one burst and the next one according to Table 10; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1,...7) with different addressing, see Table 10; Output Buffer and RTT: Enabled in Mode Registers<sup>b)</sup>; ODT Signal: stable at 0; Pattern Details: see Table 10.</p> |

a) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B

b) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT\_Nom enable: set MR1 A[9,6,2] = 011B; RTT\_Wr enable: set MR2 A[10,9] = 10B

c) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12 = 1B for Fast Exit

d) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature

e) Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for normal or 1B for extended temperature range

f) Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B



**Table 3 - IDD0 Measurement-Loop Pattern<sup>a)</sup>**

| CK, $\overline{CK}$ | CKE         | Sub-Loop | Cycle Number | Command                                                                | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | ODT | BA[2:0] | A[15:11] | A[10] | A[9:7] | A[6:3] | A[2:0] | Data <sup>b)</sup> |
|---------------------|-------------|----------|--------------|------------------------------------------------------------------------|-----------------|------------------|------------------|-----------------|-----|---------|----------|-------|--------|--------|--------|--------------------|
| toggling            | Static High | 0        | 0            | ACT                                                                    | 0               | 0                | 1                | 1               | 0   | 0       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | 1,2          | D, D                                                                   | 1               | 0                | 0                | 0               | 0   | 0       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | 3,4          | $\overline{D}, \overline{D}$                                           | 1               | 1                | 1                | 1               | 0   | 0       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | ...          | repeat pattern 1...4 until nRAS - 1, truncate if necessary             |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             |          | nRAS         | PRE                                                                    | 0               | 0                | 1                | 0               | 0   | 0       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | ...          | repeat pattern 1...4 until nRC - 1, truncate if necessary              |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             |          | 1*nRC+0      | ACT                                                                    | 0               | 0                | 1                | 1               | 0   | 0       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             |          | 1*nRC+1, 2   | D, D                                                                   | 1               | 0                | 0                | 0               | 0   | 0       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             |          | 1*nRC+3, 4   | $\overline{D}, \overline{D}$                                           | 1               | 1                | 1                | 1               | 0   | 0       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             |          | ...          | repeat pattern nRC+1...4 until 1*nRC + nRAS - 1, truncate if necessary |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             |          | 1*nRC+nRAS   | PRE                                                                    | 0               | 0                | 1                | 0               | 0   | 0       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             |          | ...          | repeat pattern nRC+1...4 until 2*nRC - 1, truncate if necessary        |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 1        | 2*nRC        | repeat Sub-Loop 0, use BA[2:0] = 1 instead                             |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 2        | 4*nRC        | repeat Sub-Loop 0, use BA[2:0] = 2 instead                             |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 3        | 6*nRC        | repeat Sub-Loop 0, use BA[2:0] = 3 instead                             |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 4        | 8*nRC        | repeat Sub-Loop 0, use BA[2:0] = 4 instead                             |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 5        | 10*nRC       | repeat Sub-Loop 0, use BA[2:0] = 5 instead                             |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 6        | 12*nRC       | repeat Sub-Loop 0, use BA[2:0] = 6 instead                             |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 7        | 14*nRC       | repeat Sub-Loop 0, use BA[2:0] = 7 instead                             |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |

a) DM must be driven LOW all the time.  $\overline{DQS}$ , DQS are MID-LEVEL

b) DQ signals are MID-LEVEL.

**Table 4 - IDD1 Measurement-Loop Pattern<sup>a)</sup>**

| CK, $\overline{CK}$ | CKE         | Sub-Loop | Cycle Number | Command                                                                 | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | ODT | BA[2:0] | A[15:11] | A[10] | A[9:7] | A[6:3] | A[2:0] | Data <sup>b)</sup> |
|---------------------|-------------|----------|--------------|-------------------------------------------------------------------------|-----------------|------------------|------------------|-----------------|-----|---------|----------|-------|--------|--------|--------|--------------------|
| toggling            | Static High | 0        | 0            | ACT                                                                     | 0               | 0                | 1                | 1               | 0   | 0       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | 1,2          | D, D                                                                    | 1               | 0                | 0                | 0               | 0   | 0       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | 3,4          | $\overline{D}$ , $\overline{D}$                                         | 1               | 1                | 1                | 1               | 0   | 0       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | ...          | repeat pattern 1...4 until nRCD - 1, truncate if necessary              |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             |          | nRCD         | RD                                                                      | 0               | 1                | 0                | 1               | 0   | 0       | 00       | 0     | 0      | 0      | 0      | 0000000            |
|                     |             |          | ...          | repeat pattern 1...4 until nRAS - 1, truncate if necessary              |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             |          | nRAS         | PRE                                                                     | 0               | 0                | 1                | 0               | 0   | 0       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | ...          | repeat pattern 1...4 until nRC - 1, truncate if necessary               |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             |          | 1*nRC+0      | ACT                                                                     | 0               | 0                | 1                | 1               | 0   | 0       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             |          | 1*nRC+1,2    | D, D                                                                    | 1               | 0                | 0                | 0               | 0   | 0       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             |          | 1*nRC+3,4    | $\overline{D}$ , $\overline{D}$                                         | 1               | 1                | 1                | 1               | 0   | 0       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             |          | ...          | repeat pattern nRC + 1,...4 until nRC + nRCD - 1, truncate if necessary |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             |          | 1*nRC+nRCD   | RD                                                                      | 0               | 1                | 0                | 1               | 0   | 0       | 00       | 0     | 0      | F      | 0      | 00110011           |
|                     |             |          | ...          | repeat pattern nRC + 1,...4 until nRC + nRAS - 1, truncate if necessary |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             |          | 1*nRC+nRAS   | PRE                                                                     | 0               | 0                | 1                | 0               | 0   | 0       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             |          | ...          | repeat pattern nRC + 1,...4 until 2* nRC - 1, truncate if necessary     |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 1        | 2*nRC        | repeat Sub-Loop 0, use BA[2:0] = 1 instead                              |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 2        | 4*nRC        | repeat Sub-Loop 0, use BA[2:0] = 2 instead                              |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 3        | 6*nRC        | repeat Sub-Loop 0, use BA[2:0] = 3 instead                              |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 4        | 8*nRC        | repeat Sub-Loop 0, use BA[2:0] = 4 instead                              |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 5        | 10*nRC       | repeat Sub-Loop 0, use BA[2:0] = 5 instead                              |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 6        | 12*nRC       | repeat Sub-Loop 0, use BA[2:0] = 6 instead                              |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 7        | 14*nRC       | repeat Sub-Loop 0, use BA[2:0] = 7 instead                              |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |

- a) DM must be driven LOW all the time.  $\overline{DQS}$ , DQS are used according to RD Commands, otherwise MID-LEVEL.  
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

**Table 5 - IDD2N and IDD3N Measurement-Loop Pattern<sup>a)</sup>**

| CK, $\overline{CK}$ | CKE         | Sub-Loop | Cycle Number | Command                                    | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | ODT | BA[2:0] | A[15:11] | A[10] | A[9:7] | A[6:3] | A[2:0] | Data <sup>b)</sup> |
|---------------------|-------------|----------|--------------|--------------------------------------------|-----------------|------------------|------------------|-----------------|-----|---------|----------|-------|--------|--------|--------|--------------------|
| toggling            | Static High | 0        | 0            | D                                          | 1               | 0                | 0                | 0               | 0   | 0       | 0        | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | 1            | D                                          | 1               | 0                | 0                | 0               | 0   | 0       | 0        | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | 2            | $\overline{D}$                             | 1               | 1                | 1                | 1               | 0   | 0       | 0        | 0     | 0      | F      | 0      | -                  |
|                     |             |          | 3            | $\overline{D}$                             | 1               | 1                | 1                | 1               | 0   | 0       | 0        | 0     | 0      | F      | 0      | -                  |
|                     |             | 1        | 4-7          | repeat Sub-Loop 0, use BA[2:0] = 1 instead |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 2        | 8-11         | repeat Sub-Loop 0, use BA[2:0] = 2 instead |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 3        | 12-15        | repeat Sub-Loop 0, use BA[2:0] = 3 instead |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 4        | 16-19        | repeat Sub-Loop 0, use BA[2:0] = 4 instead |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 5        | 20-23        | repeat Sub-Loop 0, use BA[2:0] = 5 instead |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 6        | 24-27        | repeat Sub-Loop 0, use BA[2:0] = 6 instead |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 7        | 28-31        | repeat Sub-Loop 0, use BA[2:0] = 7 instead |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |

a) DM must be driven LOW all the time.  $\overline{DQS}$ , DQS are MID-LEVEL.

b) DQ signals are MID-LEVEL.

**Table 6 - IDD2NT and IDDQ2NT Measurement-Loop Pattern<sup>a)</sup>**

| CK, $\overline{CK}$ | CKE         | Sub-Loop | Cycle Number | Command                                        | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | ODT | BA[2:0] | A[15:11] | A[10] | A[9:7] | A[6:3] | A[2:0] | Data <sup>b)</sup> |
|---------------------|-------------|----------|--------------|------------------------------------------------|-----------------|------------------|------------------|-----------------|-----|---------|----------|-------|--------|--------|--------|--------------------|
| toggling            | Static High | 0        | 0            | D                                              | 1               | 0                | 0                | 0               | 0   | 0       | 0        | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | 1            | D                                              | 1               | 0                | 0                | 0               | 0   | 0       | 0        | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | 2            | $\overline{D}$                                 | 1               | 1                | 1                | 1               | 0   | 0       | 0        | 0     | 0      | F      | 0      | -                  |
|                     |             |          | 3            | $\overline{D}$                                 | 1               | 1                | 1                | 1               | 0   | 0       | 0        | 0     | 0      | F      | 0      | -                  |
|                     |             | 1        | 4-7          | repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 2        | 8-11         | repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 2 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 3        | 12-15        | repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 4        | 16-19        | repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 4 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 5        | 20-23        | repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 6        | 24-27        | repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 7        | 28-31        | repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |

a) DM must be driven LOW all the time.  $\overline{DQS}$ , DQS are MID-LEVEL.

b) DQ signals are MID-LEVEL.

**Table 7 - IDD4R and IDDQ4R Measurement-Loop Pattern<sup>a)</sup>**

| CK, $\overline{CK}$ | CKE         | Sub-Loop | Cycle Number | Command                            | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | ODT | BA[2:0] | A[15:11] | A[10] | A[9:7] | A[6:3] | A[2:0] | Data <sup>b)</sup> |
|---------------------|-------------|----------|--------------|------------------------------------|-----------------|------------------|------------------|-----------------|-----|---------|----------|-------|--------|--------|--------|--------------------|
| toggling            | Static High | 0        | 0            | RD                                 | 0               | 1                | 0                | 1               | 0   | 0       | 00       | 0     | 0      | 0      | 0      | 00000000           |
|                     |             |          | 1            | D                                  | 1               | 0                | 0                | 0               | 0   | 0       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | 2,3          | $\overline{D}, \overline{D}$       | 1               | 1                | 1                | 1               | 0   | 0       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | 4            | RD                                 | 0               | 1                | 0                | 1               | 0   | 0       | 00       | 0     | 0      | F      | 0      | 00110011           |
|                     |             |          | 5            | D                                  | 1               | 0                | 0                | 0               | 0   | 0       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             |          | 6,7          | $\overline{D}, \overline{D}$       | 1               | 1                | 1                | 1               | 0   | 0       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             | 1        | 8-15         | repeat Sub-Loop 0, but BA[2:0] = 1 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 2        | 16-23        | repeat Sub-Loop 0, but BA[2:0] = 2 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 3        | 24-31        | repeat Sub-Loop 0, but BA[2:0] = 3 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 4        | 32-39        | repeat Sub-Loop 0, but BA[2:0] = 4 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 5        | 40-47        | repeat Sub-Loop 0, but BA[2:0] = 5 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 6        | 48-55        | repeat Sub-Loop 0, but BA[2:0] = 6 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 7        | 56-63        | repeat Sub-Loop 0, but BA[2:0] = 7 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |

a) DM must be driven LOW all the time.  $\overline{DQS}$ , DQS are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

**Table 8 - IDD4W Measurement-Loop Pattern<sup>a)</sup>**

| CK, $\overline{CK}$ | CKE         | Sub-Loop | Cycle Number | Command                            | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | ODT | BA[2:0] | A[15:11] | A[10] | A[9:7] | A[6:3] | A[2:0] | Data <sup>b)</sup> |
|---------------------|-------------|----------|--------------|------------------------------------|-----------------|------------------|------------------|-----------------|-----|---------|----------|-------|--------|--------|--------|--------------------|
| toggling            | Static High | 0        | 0            | WR                                 | 0               | 1                | 0                | 0               | 1   | 0       | 00       | 0     | 0      | 0      | 0      | 00000000           |
|                     |             |          | 1            | D                                  | 1               | 0                | 0                | 0               | 1   | 0       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | 2,3          | $\overline{D}, \overline{D}$       | 1               | 1                | 1                | 1               | 1   | 0       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | 4            | WR                                 | 0               | 1                | 0                | 0               | 1   | 0       | 00       | 0     | 0      | F      | 0      | 00110011           |
|                     |             |          | 5            | D                                  | 1               | 0                | 0                | 0               | 1   | 0       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             |          | 6,7          | $\overline{D}, \overline{D}$       | 1               | 1                | 1                | 1               | 1   | 0       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             | 1        | 8-15         | repeat Sub-Loop 0, but BA[2:0] = 1 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 2        | 16-23        | repeat Sub-Loop 0, but BA[2:0] = 2 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 3        | 24-31        | repeat Sub-Loop 0, but BA[2:0] = 3 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 4        | 32-39        | repeat Sub-Loop 0, but BA[2:0] = 4 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 5        | 40-47        | repeat Sub-Loop 0, but BA[2:0] = 5 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 6        | 48-55        | repeat Sub-Loop 0, but BA[2:0] = 6 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 7        | 56-63        | repeat Sub-Loop 0, but BA[2:0] = 7 |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |

a) DM must be driven LOW all the time.  $\overline{DQS}$ , DQS are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

**Table 9 - IDD5B Measurement-Loop Pattern<sup>a)</sup>**

| CK, $\overline{CK}$ | CKE         | Sub-Loop | Cycle Number | Command                                                    | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | ODT | BA[2:0] | A[15:11] | A[10] | A[9:7] | A[6:3] | A[2:0] | Data <sup>b)</sup> |
|---------------------|-------------|----------|--------------|------------------------------------------------------------|-----------------|------------------|------------------|-----------------|-----|---------|----------|-------|--------|--------|--------|--------------------|
| toggling            | Static High | 0        | 0            | REF                                                        | 0               | 0                | 0                | 1               | 0   | 0       | 0        | 0     | 0      | 0      | 0      | -                  |
|                     |             | 1        | 1.2          | D, D                                                       | 1               | 0                | 0                | 0               | 0   | 0       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | 3,4          | $\overline{D}, \overline{D}$                               | 1               | 1                | 1                | 1               | 0   | 0       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             |          | 5...8        | repeat cycles 1...4, but BA[2:0] = 1                       |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             |          | 9...12       | repeat cycles 1...4, but BA[2:0] = 2                       |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             |          | 13...16      | repeat cycles 1...4, but BA[2:0] = 3                       |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             |          | 17...20      | repeat cycles 1...4, but BA[2:0] = 4                       |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             |          | 21...24      | repeat cycles 1...4, but BA[2:0] = 5                       |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             |          | 25...28      | repeat cycles 1...4, but BA[2:0] = 6                       |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             |          | 29...32      | repeat cycles 1...4, but BA[2:0] = 7                       |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 2        | 33...nRFC-1  | repeat Sub-Loop 1, until nRFC - 1. Truncate, if necessary. |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |

a) DM must be driven LOW all the time.  $\overline{DQS}$ , DQS are MID-LEVEL.

b) DQ signals are MID-LEVEL.

**Table 10 - IDD7 Measurement-Loop Pattern <sup>a)</sup>**

ATTENTION! Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

| CK, $\overline{CK}$ | CKE         | Sub-Loop | Cycle Number  | Command                                                           | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | ODT | BA[2:0] | A[15:11] | A[10] | A[9:7] | A[6:3] | A[2:0] | Data <sup>b)</sup> |
|---------------------|-------------|----------|---------------|-------------------------------------------------------------------|-----------------|------------------|------------------|-----------------|-----|---------|----------|-------|--------|--------|--------|--------------------|
| toggling            | Static High | 0        | 0             | ACT                                                               | 0               | 0                | 1                | 1               | 0   | 0       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | 1             | RDA                                                               | 0               | 1                | 0                | 1               | 0   | 0       | 00       | 1     | 0      | 0      | 0      | 00000000           |
|                     |             |          | 2             | D                                                                 | 1               | 0                | 0                | 0               | 0   | 0       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | ...           | repeat above D Command until nRRD - 1                             |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 1        | nRRD          | ACT                                                               | 0               | 0                | 1                | 1               | 0   | 1       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             |          | nRRD+1        | RDA                                                               | 0               | 1                | 0                | 1               | 0   | 1       | 00       | 1     | 0      | F      | 0      | 00110011           |
|                     |             |          | nRRD+2        | D                                                                 | 1               | 0                | 0                | 0               | 0   | 1       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             |          | ...           | repeat above D Command until 2* nRRD - 1                          |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 2        | 2*nRRD        | repeat Sub-Loop 0, but BA[2:0] = 2                                |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 3        | 3*nRRD        | repeat Sub-Loop 1, but BA[2:0] = 3                                |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 4        | 4*nRRD        | D                                                                 | 1               | 0                | 0                | 0               | 0   | 3       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             |          |               | Assert and repeat above D Command until nFAW - 1, if necessary    |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 5        | nFAW          | repeat Sub-Loop 0, but BA[2:0] = 4                                |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 6        | nFAW+nRRD     | repeat Sub-Loop 1, but BA[2:0] = 5                                |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 7        | nFAW+2*nRRD   | repeat Sub-Loop 0, but BA[2:0] = 6                                |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 8        | nFAW+3*nRRD   | repeat Sub-Loop 1, but BA[2:0] = 7                                |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 9        | nFAW+4*nRRD   | D                                                                 | 1               | 0                | 0                | 0               | 0   | 7       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             |          |               | Assert and repeat above D Command until 2* nFAW - 1, if necessary |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 10       | 2*nFAW+0      | ACT                                                               | 0               | 0                | 1                | 1               | 0   | 0       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             |          | 2*nFAW+1      | RDA                                                               | 0               | 1                | 0                | 1               | 0   | 0       | 00       | 1     | 0      | F      | 0      | 00110011           |
|                     |             |          | 2*nFAW+2      | D                                                                 | 1               | 0                | 0                | 0               | 0   | 0       | 00       | 0     | 0      | F      | 0      | -                  |
|                     |             |          |               | Repeat above D Command until 2* nFAW + nRRD - 1                   |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 11       | 2*nFAW+nRRD   | ACT                                                               | 0               | 0                | 1                | 1               | 0   | 1       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          | 2*nFAW+nRRD+1 | RDA                                                               | 0               | 1                | 0                | 1               | 0   | 1       | 00       | 1     | 0      | 0      | 0      | 00000000           |
|                     |             |          | 2*nFAW+nRRD+2 | D                                                                 | 1               | 0                | 0                | 0               | 0   | 1       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          |               | Repeat above D Command until 2* nFAW + 2* nRRD - 1                |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 12       | 2*nFAW+2*nRRD | repeat Sub-Loop 10, but BA[2:0] = 2                               |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 13       | 2*nFAW+3*nRRD | repeat Sub-Loop 11, but BA[2:0] = 3                               |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 14       | 2*nFAW+4*nRRD | D                                                                 | 1               | 0                | 0                | 0               | 0   | 3       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          |               | Assert and repeat above D Command until 3* nFAW - 1, if necessary |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 15       | 3*nFAW        | repeat Sub-Loop 10, but BA[2:0] = 4                               |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 16       | 3*nFAW+nRRD   | repeat Sub-Loop 11, but BA[2:0] = 5                               |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 17       | 3*nFAW+2*nRRD | repeat Sub-Loop 10, but BA[2:0] = 6                               |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 18       | 3*nFAW+3*nRRD | repeat Sub-Loop 11, but BA[2:0] = 7                               |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |
|                     |             | 19       | 3*nFAW+4*nRRD | D                                                                 | 1               | 0                | 0                | 0               | 0   | 7       | 00       | 0     | 0      | 0      | 0      | -                  |
|                     |             |          |               | Assert and repeat above D Command until 4* nFAW - 1, if necessary |                 |                  |                  |                 |     |         |          |       |        |        |        |                    |

a) DM must be driven LOW all the time.  $\overline{DQS}$ , DQS are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

## IDD Specifications

IDD values are for full operating range of voltage and temperature unless otherwise noted.

### /DD Specification

| Speed Grade Bin | DDR3-1066 |     | DDR3-1333 |     | DDR3-1600 |     | DDR3-1866 |     | DDR3L-1066 |     | DDR3L-1333 |     | DDR3L-1600 |     | DDR3L-1866 |     | Unit |
|-----------------|-----------|-----|-----------|-----|-----------|-----|-----------|-----|------------|-----|------------|-----|------------|-----|------------|-----|------|
| Symbol          | x8        | x16 | x8        | x16 | x8        | x16 | x8        | x16 | x8         | x16 | x8         | x16 | x8         | x16 | x8         | x16 |      |
| $I_{DD0}$       | 60        | --  | 65        | --  | 70        | 80  | 50        | 90  | 30         | --  | 55         | --  | 45         | --  | 50         | --  | mA   |
| $I_{DD1}$       | 75        | --  | 80        | --  | 85        | 105 | 60        | 115 | 40         | --  | 65         | --  | 55         | --  | 60         | --  | mA   |
| $I_{DD2P0}$     | 10        | --  | 10        | --  | 10        | 10  | 12        | 10  | 10         | --  | 12         | --  | 12         | --  | 12         | --  | mA   |
| $I_{DD2P1}$     | 25        | --  | 25        | --  | 25        | 25  | 17        | 25  | 13         | --  | 20         | --  | 15         | --  | 17         | --  | mA   |
| $I_{DD2N}$      | 30        | --  | 35        | --  | 40        | 40  | 20        | 40  | 15         | --  | 30         | --  | 20         | --  | 20         | --  | mA   |
| $I_{DD2NT}$     | 35        | --  | 40        | --  | 45        | 40  | 25        | 40  | 17         | --  | 35         | --  | 25         | --  | 25         | --  | mA   |
| $I_{DD2Q}$      | 30        | --  | 35        | --  | 40        | 40  | 20        | 40  | 15         | --  | 30         | --  | 20         | --  | 20         | --  | mA   |
| $I_{DD3P}$      | 25        | --  | 25        | --  | 30        | 35  | 20        | 40  | 15         | --  | 30         | --  | 20         | --  | 20         | --  | mA   |
| $I_{DD3N}$      | 45        | --  | 50        | --  | 55        | 55  | 37        | 60  | 25         | --  | 50         | --  | 35         | --  | 37         | --  | mA   |
| $I_{DD4R}$      | 110       | --  | 125       | --  | 140       | 200 | 100       | 210 | 45         | --  | 105        | --  | 90         | --  | 100        | --  | mA   |
| $I_{DD4W}$      | 115       | --  | 135       | --  | 150       | 195 | 110       | 205 | 55         | --  | 135        | --  | 95         | --  | 110        | --  | mA   |
| $I_{DD5B}$      | 150       | --  | 160       | --  | 170       | 160 | 120       | 160 | 110        | --  | 165        | --  | 120        | --  | 120        | --  | mA   |
| $I_{DD6}$       | 10        | --  | 10        | --  | 10        | 10  | 12        | 10  | 10         | --  | 12         | --  | 12         | --  | 12         | --  | mA   |
| $I_{DD7}$       | 185       | --  | 230       | --  | 260       | 290 | 145       | 310 | 95         | --  | 195        | --  | 140        | --  | 145        | --  | mA   |

### Notes:

1. Applicable for MR2 settings A6=0 and A7=0. Temperature range for IDD6 is 0 - 85°C.

## Input/Output Capacitance

| Parameter                                                                                  | Symbol      | DDR3-1066 |      | DDR3-1333 |      | DDR3-1600 |      | DDR3-1866 |      | Units | Notes    |
|--------------------------------------------------------------------------------------------|-------------|-----------|------|-----------|------|-----------|------|-----------|------|-------|----------|
|                                                                                            |             | Min       | Max  | Min       | Max  | Min       | Max  | Min       | Max  |       |          |
| 1.35V                                                                                      |             |           |      |           |      |           |      |           |      |       |          |
| Input/output capacitance<br>(DQ,DM,DQS, $\overline{DQS}$ , TDQS, $\overline{TDQS}$ )       | CIO         | 1.4       | 2.5  | 1.4       | 2.3  | 1.4       | 2.3  | 1.4       | 2.0  | pF    | 1,2,3    |
| Input capacitance<br>(CK and $\overline{CK}$ .)                                            | CCK         | 0.8       | 1.6  | 0.8       | 1.4  | 0.8       | 1.4  | 0.8       | 1.4  | pF    | 2,3      |
| Input capacitance delta<br>(CK and $\overline{CK}$ .)                                      | CDCK        | 0         | 0.15 | 0         | 0.15 | 0         | 0.15 | 0         | 0.15 | pF    | 2,3,4    |
| Input capacitance<br>(All other input-only pins)                                           | CI          | 0.75      | 1.3  | 0.75      | 1.3  | 0.75      | 1.2  | 0.75      | 1.2  | pF    | 2,3,6    |
| Input capacitance delta<br>(DQS and $\overline{DQS}$ )                                     | CDDQS       | 0         | 0.2  | 0         | 0.15 | 0         | 0.15 | 0         | 0.15 | pF    | 2,3,5    |
| Input capacitance delta<br>(All CTRL input-only pins)                                      | CDI_CTRL    | -0.5      | 0.3  | -0.4      | 0.2  | -0.4      | 0.2  | -0.4      | 0.2  | pF    | 2,3,7,8  |
| Input capacitance delta<br>(All ADD/CMD input-only pins)                                   | CDI_ADD_CMD | -0.5      | 0.5  | -0.4      | 0.4  | -0.4      | 0.4  | -0.4      | 0.4  | pF    | 2,3,9,10 |
| Input/output capacitance delta<br>(DQ,DM,DQS, $\overline{DQS}$ , TDQS, $\overline{TDQS}$ ) | CDIO        | -0.5      | 0.3  | -0.5      | 0.3  | -0.5      | 0.3  | -0.5      | 0.3  | pF    | 2,3,11   |
| Input/output capacitance of ZQ pin                                                         | CZQ         | -         | 3    | -         | 3    | -         | 3    | -         | 3    | pF    | 2,3,12   |
| 1.5V                                                                                       |             |           |      |           |      |           |      |           |      |       |          |
| Input/output capacitance<br>(DQ,DM,DQS, $\overline{DQS}$ , TDQS, $\overline{TDQS}$ )       | CIO         | 1.5       | 2.7  | 1.5       | 2.5  | 1.5       | 2.3  | 1.4       | 2.2  | pF    | 1,2,3    |
| Input capacitance<br>(CK and $\overline{CK}$ .)                                            | CCK         | 0.8       | 1.6  | 0.8       | 1.4  | 0.8       | 1.4  | 0.8       | 1.3  | pF    | 2,3      |
| Input capacitance delta<br>(CK and $\overline{CK}$ .)                                      | CDCK        | 0         | 0.15 | 0         | 0.15 | 0         | 0.15 | 0         | 0.15 | pF    | 2,3,4    |
| Input capacitance<br>(All other input-only pins)                                           | CI          | 0.75      | 1.35 | 0.75      | 1.3  | 0.75      | 1.3  | 0.75      | 1.2  | pF    | 2,3,6    |
| Input capacitance delta<br>(DQS and $\overline{DQS}$ )                                     | CDDQS       | 0         | 0.2  | 0         | 0.15 | 0         | 0.15 | 0         | 0.15 | pF    | 2,3,5    |
| Input capacitance delta<br>(All CTRL input-only pins)                                      | CDI_CTRL    | -0.5      | 0.3  | -0.4      | 0.2  | -0.4      | 0.2  | -0.4      | 0.2  | pF    | 2,3,7,8  |
| Input capacitance delta<br>(All ADD/CMD input-only pins)                                   | CDI_ADD_CMD | -0.5      | 0.5  | -0.4      | 0.4  | -0.4      | 0.4  | -0.4      | 0.4  | pF    | 2,3,9,10 |
| Input/output capacitance delta<br>(DQ,DM,DQS, $\overline{DQS}$ , TDQS, $\overline{TDQS}$ ) | CDIO        | -0.5      | 0.3  | -0.5      | 0.3  | -0.5      | 0.3  | -0.5      | 0.3  | pF    | 2,3,11   |
| Input/output capacitance of ZQ pin                                                         | CZQ         | -         | 3    | -         | 3    | -         | 3    | -         | 3    | pF    | 2,3,12   |

### Notes:

- Although the DM, TDQS and  $\overline{TDQS}$  pins have different functions, the loading matches DQ and DQS.
- This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD, VDDQ, VSS,VSSQ applied and all other pins floating (except the pin under test, CKE,  $\overline{RESET}$  and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.
- This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
- Absolute value of CCK- $\overline{CCK}$
- Absolute value of CIO(DQS)-CIO( $\overline{DQS}$ )
- CI applies to ODT,  $\overline{CS}$ ,CKE, A0-A15, BA0-BA2, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ .
- CDI\_CTRL applies to ODT,  $\overline{CS}$  and CKE
- CDI\_CTRL=CI(CTRL)-0.5\*(CI(CLK)+CI( $\overline{CLK}$ ))
- CDI\_ADD\_CMD applies to A0-A15, BA0-BA2,  $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ .
- CDI\_ADD\_CMD=CI(ADD\_CMD) - 0.5\*(CI(CLK)+CI( $\overline{CLK}$ ))
- CDIO=CIO(DQ,DM) - 0.5\*(CIO(DQS)+CIO( $\overline{DQS}$ ))
- Maximum external load capacitance on ZQ pin: 5pF



## Standard Speed Bin

DDR3 SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

### DDR3/L-1066 Speed Bin

| Speed Bin                                |               | 1066          |           | Unit  | Note     |         |
|------------------------------------------|---------------|---------------|-----------|-------|----------|---------|
| CL - nRCD - nRP                          |               | 7-7-7         |           |       |          |         |
| Parameter                                | Symbol        | min           | max       |       |          |         |
| Internal read command to first data      | $t_{AA}$      | 13.125        | 20        | ns    |          |         |
| ACT to internal read or write delay time | $t_{RCD}$     | 13.125        | —         | ns    |          |         |
| PRE command period                       | $t_{RP}$      | 13.125        | —         | ns    |          |         |
| ACT to ACT or REF command period         | $t_{RC}$      | 50.625        | —         | ns    |          |         |
| ACT to PRE command period                | $t_{RAS}$     | 37.5          | 9 * tREFI | ns    |          |         |
| CL = 5                                   | CWL = 5       | $t_{CK(AVG)}$ | 3.0       | 3.3   | ns       | 1,2,3,4 |
|                                          | CWL = 6, 7, 8 |               | Reserved  |       | ns       | 4       |
| CL = 6                                   | CWL = 5       |               | 2.5       | 3.3   | ns       | 1,2,3   |
|                                          | CWL = 6       |               | Reserved  |       | ns       | 1,2,3,4 |
|                                          | CWL = 7, 8    |               | Reserved  |       | ns       | 4       |
| CL = 7                                   | CWL = 5       |               | Reserved  |       | ns       | 4       |
|                                          | CWL = 6       |               | 1.875     | < 2.5 | ns       | 1,2,3,4 |
|                                          | CWL = 7       |               | Reserved  |       | ns       | 1,2,3,4 |
|                                          | CWL = 8       |               | Reserved  |       | ns       | 4       |
| CL = 8                                   | CWL = 5       |               | Reserved  |       | ns       | 4       |
|                                          | CWL = 6       |               | 1.875     | < 2.5 | ns       | 1,2,3   |
|                                          | CWL = 7       |               | Reserved  |       | ns       | 1,2,3,4 |
|                                          | CWL = 8       |               | Reserved  |       | ns       | 1,2,3,4 |
| Supported CL Settings                    |               |               | 5,6,7,8   |       | $n_{CK}$ |         |
| Supported CWL Settings                   |               |               | 5, 6      |       | $n_{CK}$ |         |

## DDR3/L-1333 Speed Bin

| Speed Bin                                |               | 1333          |           | Unit     | Note     |         |
|------------------------------------------|---------------|---------------|-----------|----------|----------|---------|
| CL - nRCD - nRP                          |               | 9-9-9         |           |          |          |         |
| Parameter                                | Symbol        | min           | max       |          |          |         |
| Internal read command to first data      | $t_{AA}$      | 13.5          | 20        | ns       |          |         |
| ACT to internal read or write delay time | $t_{RCD}$     | 13.5          | —         | ns       |          |         |
| PRE command period                       | $t_{RP}$      | 13.5          | —         | ns       |          |         |
| ACT to ACT or REF command period         | $t_{RC}$      | 49.5          | —         | ns       |          |         |
| ACT to PRE command period                | $t_{RAS}$     | 36            | 9 * tREFI | ns       |          |         |
| CL = 5                                   | CWL = 5       | $t_{CK(AVG)}$ | Reserved  |          | ns       | 1,2,3,4 |
|                                          | CWL = 6, 7, 8 |               | Reserved  |          | ns       | 4       |
| CL = 6                                   | CWL = 5       |               | 2.5       | 3.3      | ns       | 1,2,3   |
|                                          | CWL = 6       |               | Reserved  |          | ns       | 1,2,3,4 |
|                                          | CWL = 7, 8    |               | Reserved  |          | ns       | 4       |
| CL = 7                                   | CWL = 5       |               | Reserved  |          | ns       | 4       |
|                                          | CWL = 6       |               | 1.875     | < 2.5    | ns       | 1,2,3,4 |
|                                          | CWL = 7       |               | Reserved  |          | ns       | 1,2,3,4 |
|                                          | CWL = 8       |               | Reserved  |          | ns       | 4       |
| CL = 8                                   | CWL = 5       |               | Reserved  |          | ns       | 4       |
|                                          | CWL = 6       |               | 1.875     | < 2.5    | ns       | 1,2,3   |
|                                          | CWL = 7       |               | Reserved  |          | ns       | 1,2,3,4 |
|                                          | CWL = 8       |               | Reserved  |          | ns       | 1,2,3,4 |
| CL = 9                                   | CWL = 5, 6    |               | Reserved  |          | ns       | 4       |
|                                          | CWL = 7       |               | 1.5       | <1.875   | ns       | 1,2,3,4 |
|                                          | CWL = 8       |               | Reserved  |          | ns       | 1,2,3,4 |
| CL = 10                                  | CWL = 5, 6    |               | Reserved  |          | ns       | 4       |
|                                          | CWL = 7       |               | 1.5       | <1.875   | ns       | 1,2,3   |
|                                          | CWL = 8       |               | Reserved  |          | ns       | 1,2,3,4 |
| Supported CL Settings                    |               |               | 6,8,9,10  |          | $n_{CK}$ |         |
| Supported CWL Settings                   |               | 5, 6, 7       |           | $n_{CK}$ |          |         |

## DDR3/L -1600 Speed Bin

| Speed Bin                                |               | 1600       |           | Unit     | Note    |
|------------------------------------------|---------------|------------|-----------|----------|---------|
| CL - nRCD - nRP                          |               | 11-11-11   |           |          |         |
| Parameter                                | Symbol        | min        | max       |          |         |
| Internal read command to first data      | $t_{AA}$      | 13.75      | 20        | ns       |         |
| ACT to internal read or write delay time | $t_{RCD}$     | 13.75      | —         | ns       |         |
| PRE command period                       | $t_{RP}$      | 13.75      | —         | ns       |         |
| ACT to ACT or REF command period         | $t_{RC}$      | 48.75      | —         | ns       |         |
| ACT to PRE command period                | $t_{RAS}$     | 35         | 9 * tREFI | ns       |         |
| CL = 5                                   | CWL = 5       | Reserved   |           | ns       | 1,2,3,4 |
|                                          | CWL = 6, 7, 8 | Reserved   |           | ns       | 4       |
| CL = 6                                   | CWL = 5       | 2.5        | 3.3       | ns       | 1,2,3   |
|                                          | CWL = 6       | Reserved   |           | ns       | 1,2,3,4 |
|                                          | CWL = 7, 8    | Reserved   |           | ns       | 4       |
| CL = 7                                   | CWL = 5       | Reserved   |           | ns       | 4       |
|                                          | CWL = 6       | Reserved   |           | ns       | 1,2,3,4 |
|                                          | CWL = 7       | Reserved   |           | ns       | 1,2,3,4 |
|                                          | CWL = 8       | Reserved   |           | ns       | 4       |
| CL = 8                                   | CWL = 5       | Reserved   |           | ns       | 4       |
|                                          | CWL = 6       | 1.875      | < 2.5     | ns       | 1,2,3   |
|                                          | CWL = 7       | Reserved   |           | ns       | 1,2,3,4 |
|                                          | CWL = 8       | Reserved   |           | ns       | 1,2,3,4 |
| CL = 9                                   | CWL = 5, 6    | Reserved   |           | ns       | 4       |
|                                          | CWL = 7       | Reserved   |           | ns       | 1,2,3,4 |
|                                          | CWL = 8       | Reserved   |           | ns       | 1,2,3,4 |
| CL = 10                                  | CWL = 5, 6    | Reserved   |           | ns       | 4       |
|                                          | CWL = 7       | 1.5        | <1.875    | ns       | 1,2,3   |
|                                          | CWL = 8       | Reserved   |           | ns       | 1,2,3,4 |
| CL = 11                                  | CWL = 5, 6,7  | Reserved   |           | ns       | 4       |
|                                          | CWL = 8       | 1.25       | <1.5      | ns       | 1,2,3   |
| Supported CL Settings                    |               | 6,8,10,11  |           | $n_{CK}$ |         |
| Supported CWL Settings                   |               | 5, 6, 7, 8 |           | $n_{CK}$ |         |

## DDR3/L-1866 Speed Bin

| Speed Bin                                |                |               | 1866             |        | Unit     | Note    |  |
|------------------------------------------|----------------|---------------|------------------|--------|----------|---------|--|
| CL - nRCD - nRP                          |                |               | 13-13-13         |        |          |         |  |
| Parameter                                | Symbol         | min           | max              |        |          |         |  |
| Internal read command to first data      | $t_{AA}$       | 13.91         | 20               | ns     |          |         |  |
| ACT to internal read or write delay time | $t_{RCD}$      | 13.91         | —                | ns     |          |         |  |
| PRE command period                       | $t_{RP}$       | 13.91         | —                | ns     |          |         |  |
| ACT to ACT or REF command period         | $t_{RC}$       | 47.91         | —                | ns     |          |         |  |
| ACT to PRE command period                | $t_{RAS}$      | 34            | 9 * tREFI        | ns     |          |         |  |
| CL = 6                                   | CWL = 5        | $t_{CK(AVG)}$ | 2.5              | 3.3    | ns       | 1,2,3   |  |
|                                          | CWL = 6        |               | Reserved         |        | ns       | 1,2,3,4 |  |
|                                          | CWL = 7, 8     |               | Reserved         |        | ns       | 4       |  |
| CL = 7                                   | CWL = 5        |               | Reserved         |        | ns       | 4       |  |
|                                          | CWL = 6        |               | 1.875            | < 2.5  | ns       | 1,2,3,4 |  |
|                                          | CWL = 7        |               | Reserved         |        | ns       | 1,2,3,4 |  |
|                                          | CWL = 8        |               | Reserved         |        | ns       | 4       |  |
| CL = 8                                   | CWL = 5        |               | Reserved         |        | ns       | 4       |  |
|                                          | CWL = 6        |               | 1.875            | < 2.5  | ns       | 1,2,3   |  |
|                                          | CWL = 7        |               | Reserved         |        | ns       | 1,2,3,4 |  |
|                                          | CWL = 8        |               | Reserved         |        | ns       | 1,2,3,4 |  |
| CL = 9                                   | CWL = 5, 6     |               | Reserved         |        | ns       | 4       |  |
|                                          | CWL = 7        |               | 1.5              | <1.875 | ns       | 1,2,3,4 |  |
|                                          | CWL = 8        |               | Reserved         |        | ns       | 1,2,3,4 |  |
| CL = 10                                  | CWL = 5, 6     |               | Reserved         |        | ns       | 4       |  |
|                                          | CWL = 7        |               | 1.5              | <1.875 | ns       | 1,2,3   |  |
|                                          | CWL = 8        |               | Reserved         |        | ns       | 1,2,3,4 |  |
| CL = 11                                  | CWL = 5, 6,7   |               | Reserved         |        | ns       | 4       |  |
|                                          | CWL = 8        |               | 1.25             | <1.5   | ns       | 1,2,3   |  |
|                                          | CWL = 9        |               | Reserved         |        | ns       | 4       |  |
| CL = 12                                  | CWL = 5, 6,7,8 |               | Reserved         |        | ns       | 4       |  |
|                                          | CWL = 9        |               | Reserved         |        | ns       | 4       |  |
| CL = 13                                  | CWL = 5, 6,7,8 |               | Reserved         |        | ns       | 4       |  |
|                                          | CWL = 9        |               | 1.071            | <1.25  | ns       | 1,2,3   |  |
| Supported CL Settings                    |                |               | 6,7,8,9,10,11,13 |        | $n_{CK}$ |         |  |
| Supported CWL Settings                   |                |               | 5, 6, 7, 8,9     |        | $n_{CK}$ |         |  |

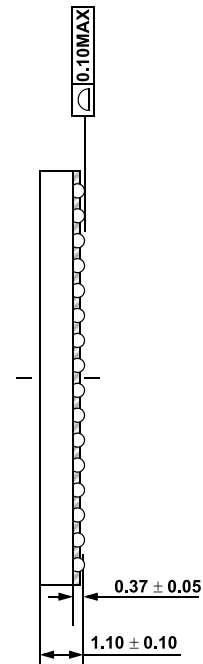
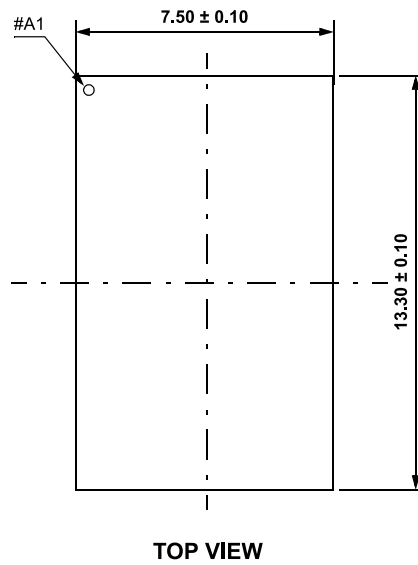
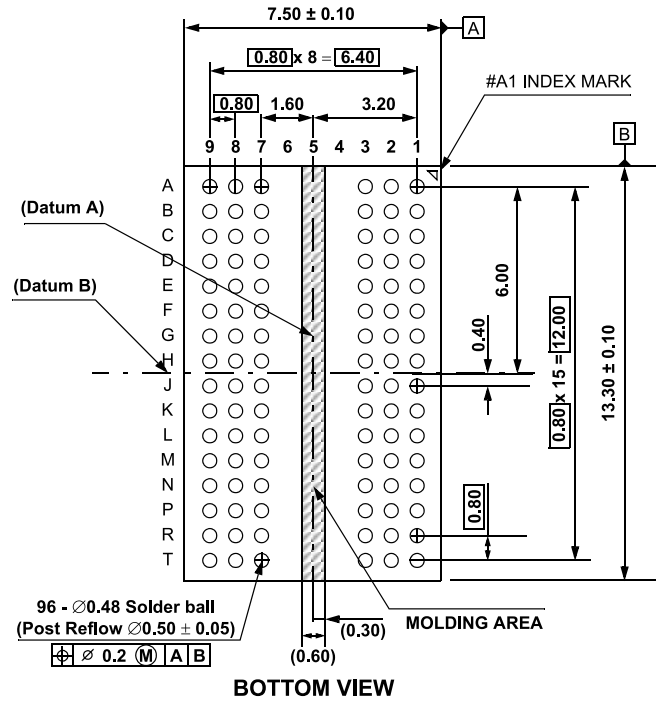
**Speed Bin Table Notes**

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating  $CL [nCK] = tAA [ns] / tCK(AVG) [ns]$ , rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation.
3. tCK(AVG).MAX limits: Calculate  $tCK(AVG) = tAA.MAX / CL SELECTED$  and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to DECUN DIMM data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

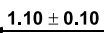
## Package Dimensions

### 96-BALL DDR SDRAM (7.5x13.3mm, FA)

Units : Millimeters



## Units : Millimeters



## Units : Millimeters

